TMC2081

Digital Video Mixer

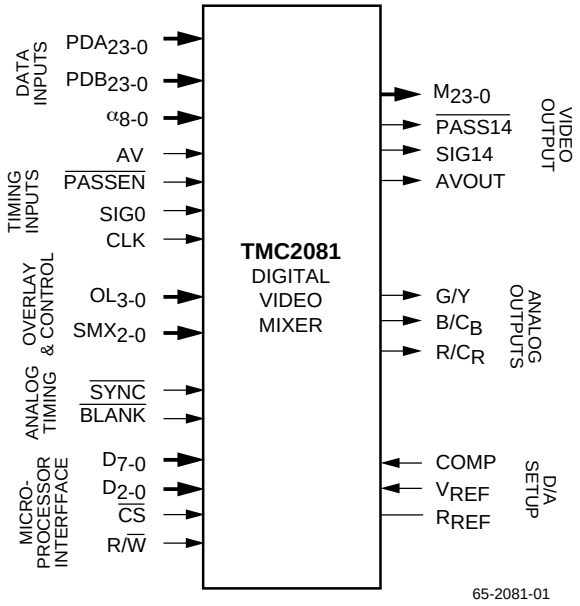
Features

- Mixes 24//16-bit GBR/YC_BC_R444//YC_BC_R422 and 8-bit color-index sources
- 24//16-bit GBR/YC_BC_R444//YC_BC_R422 output
- 255-step proportional mixing via α_{7-0} inputs
- 256-step mixing with α_{8-0} for α=100h unity gain
- 256 x 8-bit look-up table on α channel
- Lap-dissolve and fade effects
- α and crosspoint controls for soft and color-border wipe generation
- Mask register and three 256 x 8 bypassable CLUTs with overlay on A-channel
- Analog preview output with sync on Green/Y
- D/A power-down modes
- Single +5 volt power supply operation
- Pin compatible with TMC22080 Digital Mixer

Applications

- Mixing computer graphics and live video
- Lap-dissolve between video sources
- Fade to black or to user-selectable fill color
- Window/wipe processing

Logic Symbol



65-2081-01

Description

The TMC2081 is a Digital Video Mixer that performs

$\mathbf{M} = (\alpha) \mathbf{V}_1 + (1-\alpha) \mathbf{V}_2 \quad (\text{for } 0 \le \alpha \le 1)$

cross-fading at speeds faster than 40 Mpps proportionally controlled by a 9-bit α-channel input. Variable rate dissolves and fades may be implementedwith unity gain at the α end-points. With the α-Look-Up Table (αLUT), mixing may be controlled by a single bit of the α-channel input. Setup is via a microprocessor interface.

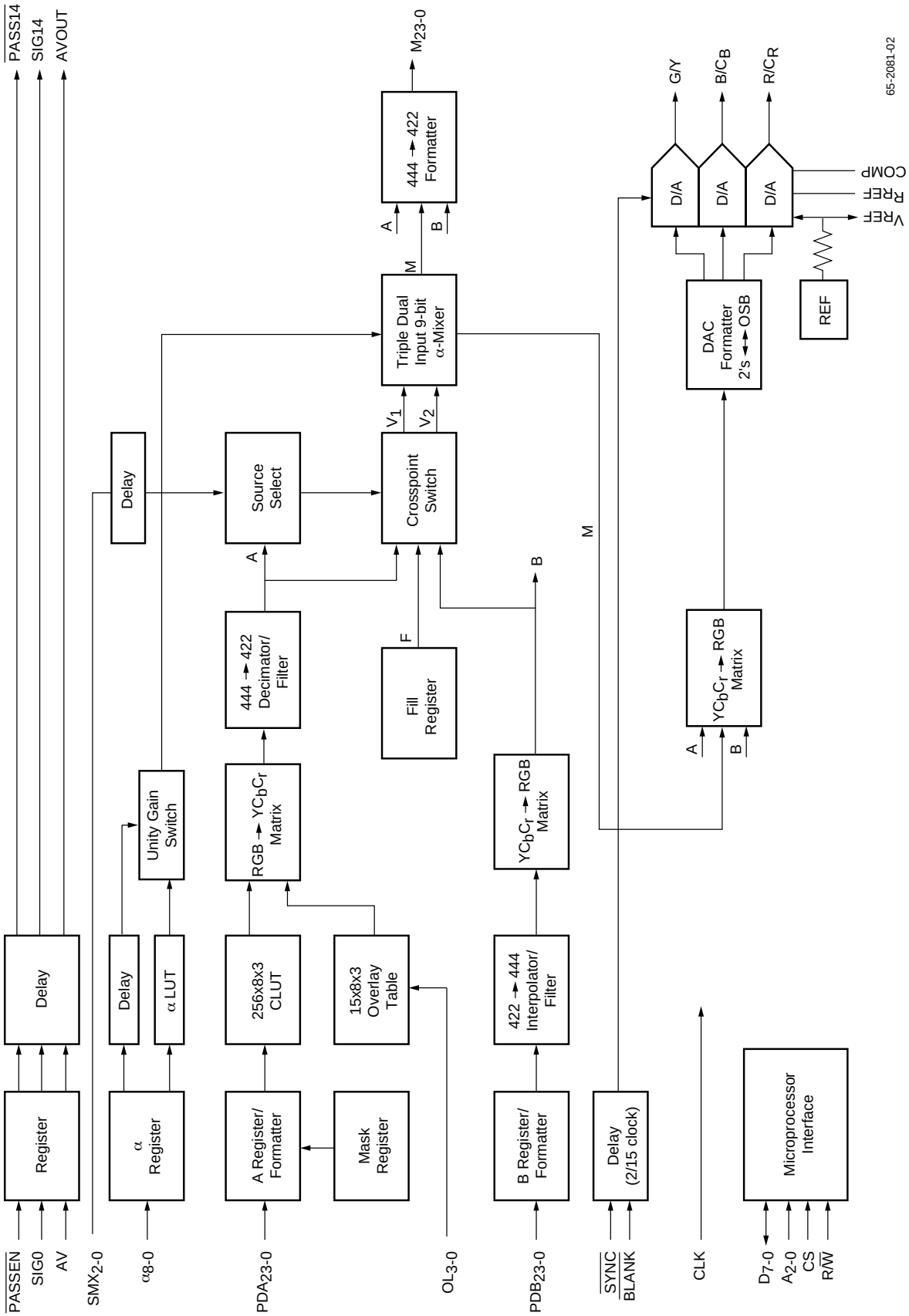
Supported video formats are 24-bit GBR, YC_BC_R444, and 16-bit YC_BC_R422 component video. Dissimilar pixel formats may be mixed using on-chip interpolation and decimation filters and GBR/YC_BC_R and YC_BC_R/GBR color-space conversion matrices.

An additional format accepted by the A-channel is 8-bit color-indexed pixel data which addresses three bypassable 256 x 8 color look-up tables (CLUTs). A 15 color overlay palette and a 24-bit fill register are also included.

Digital and Analog outputs may be programmed to view either mixer inputs, V_1 or V_2 or mixer output, M.

Packaged in a 128-lead plastic metric quad flat-pack (MQFP), the TMC2081 is fabricated with a sub-micron CMOS process. Performance is guaranteed over the commercial, 0°C to 70°C temperature range.

Block Diagram



Functional Description

The TMC2081 is a monolithic digital video processor that proportionally mixes digital video in GBR, YC_BC_R, or color-index formats. Some of the variety of input and output data format combinations are shown in Table 1.

The A-channel data path has transformation circuits that can look up 24-bit GBR values from 8-bit color-index inputs, convert GBR-to-YC_BC_R format, and decimate YC_BC_R444 to YC_BC_R422. The B-channel path includes circuits that convert YC_BC_R to GBR and interpolate YC_BC_R422 to YC_BC_R444. Prior to mixing, incoming pixel data streams must be converted to matching formats by setting the A and B channel control registers.

Data enters the TMC2081 through the PDA_{23-0}, PDB_{23-0}, α_{8-0}, and OL_{3-0} ports. Data and video controls ($\overline{PASSEN}$ and AV) are simultaneously registered on the rising edge of PXCLK. Pipeline latency is 14 clock cycles to the mixed digital video output.

Although PDA_{23-0}, PDB_{23-0}, and M_{23-0} data formats may be different, V_1 and V_2 data formats at the α-Mixer input must be matched: unsigned magnitude for GBR and Y components; 2's complement for C_B and C_R components.

Data formats converted within the TMC2081 are determined by the control bits programmed into the internal registers.

Output format may be GBR, YC_BC_R444 or YC_BC_R422. Either crosspoint switch input, A and B or the Mixer output may be selected at the M_{23-0} port. Table 2, Table 3 and Table 4 show examples of the M_{23-0} output for 9-bit α-mixing. In Table 3, C_BC_R is accepted at the C_B input. Table 4 exemplifies format
conversion.

Mixer output and inputs may be previewed by three video D/A converters. Analog outputs may be either GBR or YC_BC_R.

For initialization and control, internal registers and tables may be accessed through a microprocessor interface.

Power may be conserved by disabling the D/A converters or sections of the TMC2081 via internal Control Registers. In the latter mode, the microprocessor interface remains active and Control Register settings are retained but CLUT locations are not accessible.

Table 1. Input and Output Data Format Examples

A Input Format	B Input Format	A CLUT	A GBR-YC_BC_R	A Decimate	B Interpolate	B YC_BC_R-GBR	M Format	M Output Format
YC_BC_R444	YC_BC_R444	Bypass	Bypass	Bypass	Bypass	Bypass	Low	YC_BC_R444
YC_BC_R444	YC_BC_R422	Bypass	Bypass	Bypass	Enable	Bypass	Low	YC_BC_R444
YC_BC_R444	YC_BC_R422	Bypass	Bypass	Enable	Bypass	Bypass	High	YC_BC_R422
YC_BC_R422	YC_BC_R422	Bypass	Bypass	Bypass	Bypass	Bypass	High	YC_BC_R422
YC_BC_R422	YC_BC_R422	Bypass	Bypass	Bypass	Bypass	Bypass	Low	YC_BC_R444
GBR, CI	YC_BC_R444	Enable	Bypass	Bypass	Bypass	Enable	Low	GBR
GBR, CI	YC_BC_R444	Enable	Enable	Bypass	Bypass	Bypass	Low	YC_BC_R444
GBR, CI	YC_BC_R422	Enable	Bypass	Bypass	Enable	Enable	Low	GBR
GBR, CI	YC_BC_R422	Enable	Enable	Enable	Bypass	Bypass	High	YC_BC_R422
GBR, CI	GBR	Enable	Bypass	Bypass	Bypass	Bypass	Low	GBR

Table 2. GBR Mixing Example (9-bit α)

α (hex)	PDA (hex)			PDB (hex)			M (hex)		
	G	B	R	G	B	R	G	B	R
000	BB	CC	AA	EE	FF	DD	EE	FF	DD
040	BB	CC	AA	EE	FF	DD	E1	F2	D0
080	BB	CC	AA	EE	FF	DD	D5	E6	C4
100	BB	CC	AA	EE	FF	DD	BB	CC	AA

Table 3. YC_BC_R422 Mixing Example (C_B and C_R in 2's Complement)

α	PDA (hex)			PDB (hex)			M (hex)		
(hex)	Y	C_B	C_R	Y	C_B	C_R	Y	C_B	C_R
40	10	F4	XX	20	4	XX	1C	00	00
80	10	F4	XX	20	4	XX	18	00	00
40	10	F4	XX	20	4	XX	1C	00	00
40	10	FE	XX	20	2	XX	1C	01	00
A0	30	60	XX	40	70	XX	36	66	00
B0	30	80	XX	40	90	XX	35	86	00
A0	30	C0	XX	40	D0	XX	36	C6	00
B0	30	E0	XX	40	F0	XX	35	E5	00

Table 4. YC_BC_R422-to-YC_BC_R444 Mixing Example

α	PDA (hex)			PDB (hex)			M (hex)		
(hex)	Y	C_B	C_R	Y	C_B	C_R	Y	C_B	C_R
40	10	F4	XX	20	4	XX	1C	00	00
40	10	F4	XX	20	4	XX	1C	00	00
40	10	F4	XX	20	4	XX	1C	00	01
40	10	FE	XX	20	2	XX	1C	00	01
A0	30	60	XX	40	70	XX	36	66	86
B0	30	80	XX	40	90	XX	35	66	86
A0	30	C0	XX	40	D0	XX	36	C6	E5
B0	30	E0	XX	40	F0	XX	35	C6	E5

Input Formats

Data is accepted by PDA and PDB channels in one pair of the following formats:

1. YC_BC_R444
2. YC_BC_R422
3. GBR
4. 8-bit color-index mapped to a palette of 256x256x256 colors. (A-channel only)

Details of bits assignments are shown in Figure 1. Pixel Data Formats with the expected data ranges are shown in Table 5.

Table 5. YC_BC_R and GBR Data Types and Ranges

Signal	Min.	Max.	Format
GBR	0	255	Unsigned Binary
Y	16	235	Unsigned Binary
C_BC_R	-112	+112	2's Complement
			Offset Binary

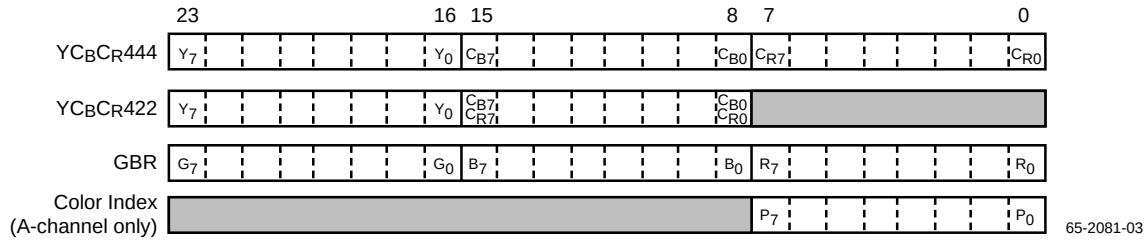


Figure 1. Pixel Data Formats

A-Channel Operation

A-channel pixel data, PDA, is registered on the rising edge of CLK. C_BC_R data is either passed or format converted (from offset binary to 2's complement) by MSB inversion. 16-bit YC_BC_R422 data is converted to 24-bit YC_BC_R data by pixel replication of C_BC_R data. Each of the three A channel bytes is logically-ANDed with the contents of the Mask Register.

The CLUT in the A-channel pixel data path comprises three 256-word x 8-bit sections. When the CLUT is enabled, pixel data addresses the CLUT, which outputs the address contents for subsequent processing. The CLUT may also be bypassed, passing incoming pixel data directly to subsequent circuits.

For 24-bit GBR operation, each of the 256-word by 8-bit CLUTs is independently addressed by green, blue, and red bytes from PDA_{23-0}. For Color-index operation, each of the 256 x 8 CLUTs is addressed by the same pixel data from PDA_{7-0}.

CLUT locations may hold GBR or YC_BC_R color values. V_1 and V_2 mixer input formats must match CLUT formats.

The PDA overlay palette is addressed by four Overlay inputs, OL_{3-0} and is enabled via the Control Register. Each valid Overlay address produces one of 15 24-bit colors selected from stored 8-bit red, green, and blue values. If all four overlay inputs are LOW, CLUT data is selected. If any overlay input is HIGH, OL_{3-0} is decoded into the corresponding color which is selected at the RGB/YC_BC_R matrix. OL_{3-0} may be changed on a pixel-by-pixel basis.

Table 6. A-Channel GBR-to-YC_BC_R Mapping for Fully-Saturated Colors

Color	Input Values			Output Values		
	R	G	B	Y	C_B	C_R
White	255	255	255	235	0	0
Yellow	255	255	0	210	-112	18
Cyan	0	255	255	169	38	-112
Green	0	255	0	144	-74	-94
Magenta	255	0	255	106	74	94
Red	255	0	0	81	-38	112
Blue	0	0	255	41	112	-18
Black	0	0	0	16	0	0

Table 7. B-Channel YC_BC_R-GBR Mapping for Fully-Saturated Colors

Color	Input Values			Output Values		
	Y	C_B	C_R	R	G	B
White	235	0	0	255	255	255
Yellow	210	-112	18	255	255	0
Cyan	169	38	-112	0	255	255
Green	144	-74	-94	0	255	0
Magenta	106	74	94	255	0	255
Red	81	-38	112	255	0	0
Blue	41	112	-18	0	0	255
Black	16	0	0	0	0	0

B-Channel Operation

YC_BC_R444, YC_BC_R422, or GBR are accepted by the B-channel. PDB_{23-0} pixel data is registered on the rising edge of CLK. 16-bit YC_BC_R422 data is converted to 24-bit YC_BC_R444 data by pixel replication of C_BC_R data in the Register/Formatter.

24-bit data is passed to an interpolation filter followed by a color-space converter to ensure that the B-channel data format matches that of the A-channel prior to mixing. Table 1 illustrates the setup of color-space converters, decimation, and interpolation filters. Pipeline latencies of the A and B-channels are matched.

Interpolation and Decimation Filters

Digital interpolation and decimation filters in the A- and B-channels suppress unwanted artifacts in the chrominance components. Maximum passband attenuation is 0.06 dB. Minimum stopband rejection is 41 dB.

When the input format is YC_BC_R422, the incoming pixel following AV transitioning HIGH is assumed to be the C_B pixel. (See Figure 11.)

α-Channel Operation

Nine bits of α data are registered on a pixel-by-pixel basis from α_{8-0}. Either 9-bit or 8-bit α values can be selected by setting Control Register Bit αGAIN. Table 8 shows the differences between the 8-bit and 9-bit gain settings for a 0FF input.

Bits α_{7-0} address a 256 x 8-bit lookup table (αLUT). The αLUT may be used to redefine the function of incoming α data for special effects or low resolution dissolves and fades.

Bit α_8 controls a unity gain switch. If $\alpha_8 = 1$, then α is set to unity gain. α_8 functions independently of the α gain bit register 0. For 8-bit α mixing, set $\alpha_8 = 0$.

By setting control register bit αLUTEN = 0, the αLUT may be completely bypassed, allowing α_{8-0} to directly control the mixing of A, B and F. αLUT locations may be accessed via the D_{7-0} microprocessor port.

Table 8. Alpha Channel Gains

α value (hex)	8-bit Gain	9-bit Gain
000	0/256	0/256
001	1/256	1/256
. .		
07F	127/256	127/256
080	128/256	128/256
. .		
0FE	254/256	254/256
0FF	256/256	255/256
100	256/256	256/256
1XX	256/256	256/256

Fill Color Registers

Three registers, 03, 04, and 05, store a solid fill color, F. Either GBR values or YC_BC_R values may be stored but the format must match the data format of the A- and B-channels at the input to the crosspoint switch.

Fill color registers are accessed through the D_{7-0} microprocessor port. Fill color may be used as an alternative video source for fades.

α-Mixer

There are three sources of data for the mixer: A-channel pixels, B-channel pixels, and the stored fill color, F. One pair of inputs, either AB, BF or FA are selected by the Crosspoint Switch to be passed to the V_1 and V_2 inputs of the α-Mixer. Prior to mixing, V_1 and V_2 data formats must be matched (see Table 1).

Within the α-Mixer are three dual input 9-bit mixers which mix each of the component channels of V_1 and V_2. By varying the value on the α-channel from 000_h to 100_h, the Mixer performs a 256-step transition from one digital video source to the other.

Six dissolve transitions are supported: A-to-B, A-to-F, B-to-A, B-to-F, F-to-A, and F-to-B. Type of dissolve is selected by directing the A-, B-, or F pixels to the V_1 or V_2 mixer input via the ABF Crosspoint Switch. This is done either by internal Control Registers via the microprocessor port or directly through the SMX_{2-0} inputs. SMX_{2-0} input pins are enabled via SMX Control Register bits. When enabled, SMX_{2-0} directly control the ABF Crosspoint Multiplexer on a pixel-by-pixel basis, for externally derived wipe patterns.

Rate of dissolve is controlled directly through the α-channel. Transfer function of the mixer is:

$$M = (\alpha) V_1 + (1-\alpha) V_2$$

where V_1 and V_2 are two of the three inputs A, B or F selected by the crosspoint switch.

For an A-to-B dissolve transition, as the value of the eight LSBs of the α-channel change from 00_h to FF_h, (or 000_h to 100_h in the 9-bit mode), an increasing level of A-channel contribution and a decreasing level of B-channel contribution becomes evident at the output, M.

Bit α_8 of the α-channel can correct for the 255/256 gain factor in the A-channel that occurs when the 8-bit α value is FF_h. When α_8 =1, bits α_{7-0} are ignored, A-channel gain is set to 256/256 and B-channel gain is set to 0/256.

Modified transfer functions may be selected for background/foreground and drop-shadow effects by programming control register bits, MIXTFN.

A Foreground Key may be created such that:

$$M = (\alpha) V_1$$

A Background Key may be created such that:

$$M = (\alpha) V_1 + V_2$$

By using foreground and background mixers in series, drop shadow effects can be implemented.

α may change at pixel rates up to 40 Mpps on a pixel-by-pixel basis, allowing smooth transitions from one video source to another. Transition time interval may vary from many frames to only a few or a single pixel depending upon the α-channel data rate.

α_8 may be used like a key input. Either unity gain V_1 or $(1-\alpha)V_2$ may be selected. A- and B-channel pixels may be mixed by switching α_8 on a pixel-by-pixel basis. Pipeline latencies of the α-, A- and B-channels are matched.

Passing of Non-Pixel Data

In the PASSON mode, the TMC2081 is transparent to data accepted during the $\overline{PASSEN}$ = LOW period (see Figure 10 and Figure 11). Either PDA or PDB data may be selected to pass on reference signals containing time codes, subcarrier phase and frequency data from upstream video processors.

Digital Outputs

Data at the M_{23-0} output port, may be selected from either the mixer or, for digital preview, the A or B crosspoint switch inputs.

The 444-to-422 formatter may be bypassed for 24-bit output. To convert 24-bit YC_BC_R data to the 16-bit YC_BC_R422 format, the formatter needs to be enabled.

Except for color index, all data formats shown in Figure 1 are available:

- YC_BC_R444
- YC_BC_R422
- GBR

M_{23-0} bits are clocked synchronously with the rising edge of CLK. M_{23-0} data outputs may be disabled to a high-impedance state by setting the MOUT Control Register bit LOW.

Analog Preview

Either crosspoint switch input (A or B) or the mixed pixel data output (M_{23-0}) can be monitored by D/A con-verters. D/A outputs may be either YC_BC_R or GBR. A YC_BC_R-to-GBR matrix prior to the D/A converters can be selected for color-space conversion.

To view A or B data originating in the C_BC_R format, the DACFRM Control Register bit must be set to convert 2's-complement data to the offset binary format.

With the DACSLP bit, D/A converters can be powered down and with the DACOVL bit, the D/A overlay RAM can be powered down.

D/A Converter Outputs

Each D/A converter comprises an array of current sources referenced to V_{DD} and controlled by the data, $\overline{BLANK}$, and $\overline{SYNC}$ inputs. When $\overline{BLANK}$ = HIGH, the SETUP Control Register bit determines if a pedestal is activated. With nominal R_{REF} and V_{REF}, outputs match SMPTE 170M levels when terminated with a 37.5Ω resistive load (75Ω at the source and destination). By doubling R_{REF}, a 75Ω load can be accommodated.

Full scale current is set by an external resistor, R_{SET}, connected between the R_{REF} pin and A_{GND} and the reference voltage, V_{REF}. V_{REF} may be derived from either a 1.235 volt internal source or an external voltage reference connected to V_{REF}.

Nominal outputs (see Figure 2 and Figure 3) are expressed in Current Units (IU) where 1 IU is equivalent to the current activated by one unit of D/A input data (Gdata/Ydata, Bdata/$C_R$data, or Rdata/$C_B$data). SETUP = HIGH activates a 21 IU pedestal when $\overline{BLANK}$= H. $\overline{SYNC}$ = LOW disables a 110 IU sync pulse. SETUP is programmed through Register 7 bit 2.

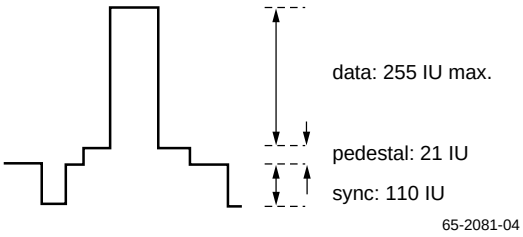


Figure 2. GBR/Y DAC Output Levels in Current Units

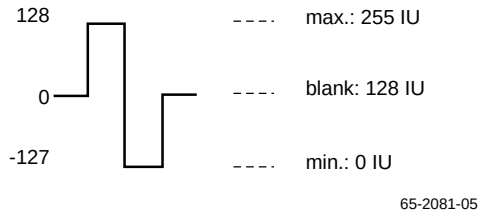


Figure 3. C_BC_R DAC Output Levels in Current Units

To translate IUs to millivolts, V_{REF} and R_{SET} must be set to the correct values, nominally V_{REF} = 1.235 volt and R_{SET} = 681 ohms. In each table below, G and the Y outputs have been normalized to 1000 mV with Data = 255.

Since V_{REF} and R_{REF} are common to all D/A converters, B and R full scale outputs track G. C_B C_R full scale outputs track Y. R_{REF} may be trimmed to set the G or Y full scale voltage to 1000 mV.

In the equations for the GBR and YC_BC_R outputs that follow, symbols are defined as:

+ = plus

* = multiply

& = logical AND

! = logical complement

GBR Output

Expressed in IUs, the GBR transformation from data to current is as follows:

G = (Gdata + SETUP * 21) & $\overline{BLANK}$ + $\overline{SYNC}$ * 110

B = (Bdata + SETUP * 21) & $\overline{BLANK}$

R = (Rdata + SETUP * 21) & $\overline{BLANK}$

Sample outputs are listed in Table 9 and Table 10.

Table 9. GBR DAC Transfer Characteristic without Pedestal (SETUP = L)

D/A Input Data	$\overline{SYNC}$	$\overline{BLANK}$	G		B or R	
			IU	mV	IU	mV
255	1	1	365	1000	255	699
128	1	1	238	652	128	351
0	1	1	110	301	0	0
X	1	0	110	301	0	0
X	0	0	0	0	0	0
128	0	1	128	351	128	351

Table 10. GBR DAC Transfer Characteristic with Pedestal (SETUP = H)

D/A Input Data	$\overline{SYNC}$	$\overline{BLANK}$	G		B or R	
			IU	mV	IU	mV
255	1	1	386	1000	276	715
128	1	1	259	671	149	386
0	1	1	131	339	21	54
X	1	0	110	285	0	0
X	0	0	0	0	0	0
128	0	1	149	386	149	386

YC_BC_R Output

Data inputs are unsigned Ydata and offset-binary format $C_B$data and $C_R$data. $\overline{BLANK}$ = L sets C_B and C_R outputs to 128, the value for zero chrominance data. YC_BC_R transfer equations are:

$Y = (Ydata + SETUP * 21) \& \overline{BLANK} + \overline{SYNC} * 110$

$C_B = (Cdata + SETUP * 21) \& \overline{BLANK} + 128 \& !\overline{BLANK}$

$C_R = (Cdata + SETUP * 21) \& \overline{BLANK} + 128 \& !\overline{BLANK}$

Sample outputs are listed in Table 11 and Table 12.

Table 11. YCrCb DAC Transfer Characteristic without Pedestal (SETUP = L)

D/A Input Data	$\overline{SYNC}$	$\overline{BLANK}$	Y		C_B or C_R	
			IU	mV	IU	mV
255	1	1	365	1000	255	699
128	1	1	238	652	128.	351
64	1	1	174	477	64	175
0	1	1	110	301	0	0
X	1	0	110	301	128	351
X	0	0	0	0	128	351
64	0	1	64	175	64	175

Table 12. YCrCb DAC Transfer Characteristic with Pedestal (SETUP = H)

D/A Data	$\overline{SYNC}$	$\overline{BLANK}$	Y		C_B or C_R	
			IU	mV	IU	mV
255	1	1	386	1000	276	715
128	1	1	259	670	149	386
64	1	1	195	505	85	220
0	1	1	131	339	21	54
X	1	0	110	285	149	386
X	0	0	0	0	149	386
64	0	1	85	220	85	220

Dissolve and Crossfade Operation

Video transitions such as dissolve and fades may be executed by direct α-channel control. Rate and start time for the transition depends entirely upon the value of the $\alpha_{8\text{-}0}$ inputs. Transitions may be executed as quickly or slowly as values are presented to the α-channel. Transitions may remain partially executed by keeping α-values constant.

It is possible to mix modes, bringing data in either 444 or 422 format and outputting data in 422 or 444 format.

In the 444/444 mode (see Figure 7), α is applied to each YC_BC_R or GBR pixel pair at the input of the mixer. The YC_BC_R444 output is mixed at the full α rate.

In the 422/422 mode (see Figure 8), α mixes the Y component of incoming PDA and PDB pixels. Only odd indexed α values mix C_BC_R components. α-values applied to C_BC_R change synchronously with C_B data. Consequently, full bandwidth α data is applied to the luminance channel but the chrominance channel α values are decimated by dropping the even values that are synchronous with C_R data.

In the 422/444 mode (see Figure 9), YC_BC_R422 data is accepted at the PDA and PDB port but the output at the $M_{23\text{-}0}$ port is YC_BC_R444. α may change from pixel-to-pixel with mixing at the $M_{23\text{-}0}$ outputs tracking both Y and C_BC_R. Although odd values of C_B and C_R are repeated at half the pixel rate, α transitions are applied to C_B and C_R at the pixel rate.

Microprocessor Interface

Internal Control Registers, CLUT, αLUT, and the overlay palette are accessed through a bi-directional microprocessor port, $D_{7\text{-}0}$. Table 13 shows how address bits, $A_{2\text{-}0}$, select the registers to be accessed.

Table 13. Microprocessor Port Address Map

$A_{2\text{-}0}$	Action
000	RAM Address Register for CLUT, αLUT, and overlay palette for write operations
001	Directs RAM R/W operations selected by the two MSBs of Control Address Register
010	Reserved
011	RAM Address Register for CLUT, αLUT, and overlay palette for read operations
100	Reserved
101	Directs Control Register R/W operations selected by the four LSBs of the Control Address Register
110	Mask Register (Default: Load with FF)
111	Control Address Register

As shown in Table 14, to access a control register, Control Address Register bits D_{3-0} must be set to specify one of the nine control registers shown in Table 17. For access to LUTs and Overlay palettes, Control Address Register bits D_{7-6} must be set to select the address of one of the four RAMs shown in Table 14.

Table 14. Control Address Register Bit Definitions

RAM Select		Reserved		Control Register Address			
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
00		A-channel CLUT					
01		A-channel Overlay palette					
10		Reserved					
11		αLUT					

Figure 4 and Figure 5 show the microprocessor port read and write timing cycles. Table 15 shows the Control Register read and write sequences.

When loading or reading look-up tables or the overlay palette, with the exception of α-LUT write, the address pointer is auto-incremented after each read or write operation. For α-LUT write, the address pointer is pre-incremented, so that the address must be set one address before the required address. For α-LUT read, the address pointer is post-incremented.

When accessing the A-channel CLUT, or A-channel Overlay palette, each address location must be written/read three consecutive times for red (R/C_R), green (G/Y), and blue (B/C_B) data. After accessing the blue data, the address pointer auto-increments.

In Table 16, note that:

1. To read the α-LUT, Control Register 06h, bit 5 must be set to enable the α-LUT.
2. To read the CLUT and Overlay Table, Control Register 00h, bit 4 (CLUT) must be set to enable both the CLUT and Overlay Table.
3. Data may be written to the CLUT or αLUT with Control Register bits set to enable or bypass.
4. When writing to the α-LUT, the address pre-increments. The address pointer is set to FFh, one address before address 00h.
5. Load mask register to pass PDA data.

Power and Ground

The TMC2081 operates from a single +5 Volt power supply. Multiple power and ground pins are assigned and must be connected.

Table 15. Control Register Read/Write Sequences

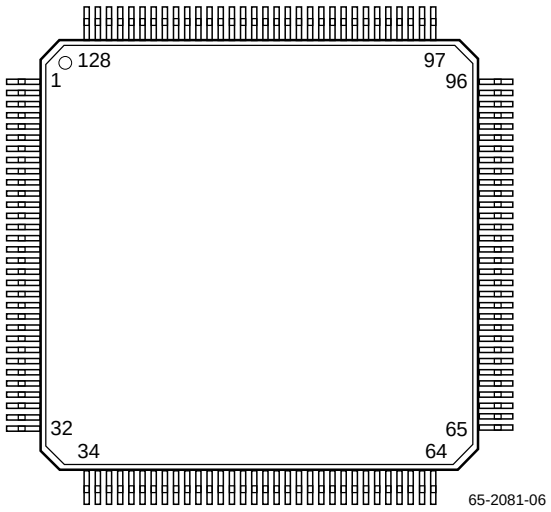
Step	$R/\overline{W}$	A_{2-0}	D_{7-0}	Function
Write to all Control Registers				
1	0	111	x0	Writes 0 to Address Control Register (selects the A-channel Control Register)
2	0	101	aa	Writes aa into A-channel Control Register
.	. .	. .	. .	Repeat steps 1 and 2 incrementing data to Address Control Register
15	0	111	07	Writes 07 to Address Control Register (selects the D/A Control Register)
16	0	101	bb	Writes bb into D/A Control Register
Read/Modify/Write Mixer Control Register				
1	0	111	x2	Writes 02 to Address Control Register (selects the Mixer Control Register)
2	1	101	aa	Mixer Control Register contents, aa, available on D_{7-0}.
.	. .	. .	. .	System modifies aa to get bb.
3	0	101	bb	Writes bb into Mixer Control Register

Table 16. CLUT Read/Write Sequences

Step	R/$\overline{W}$	A_{2-0}	D_{7-0}	Function
Write Entire A-Channel CLUT from Address 00				
1	0	111	0x	Selects A-CLUT for write.
2	0	000	00	Presets RAM Address Register to 00.
3	0	001	r0	r0 written into red (R/C_R) CLUT address 00.
4	0	001	g0	g0 written into green (G/Y) CLUT address 00.
5	0	001	b0	b0 written into blue (B/C_B) CLUT address 00.
.	. .	. .	. .	repeat steps 3,4,5 until A-CLUT is full.
768	0	001	r255	r255 written into red (R/C_R) CLUT address FF.
769	0	001	g255	g255 written into green (G/Y) CLUT address FF.
770	0	001	b255	b255 written into blue (B/C_B) CLUT address FF.
Write GBR Data to A-Overlay Location Address				
1	0	111	4x	Select A-channel Overlay.
2	0	000	a_n	Write a_n into RAM Address Register.
3	0	001	r_n	r_n written into red (R/C_R) CLUT address.
4	0	001	g_n	g_n written into green (G/Y) CLUT address.
5	0	001	b_n	b_n written into blue (B/C_B) CLUT address.
Write all αLUT Locations starting from 00				
1	0	111	Cx	Select αLUT.
2	0	000	FF	Write FF into RAM Address Register (sets address to FF for pre-increment).
3	0	001	$\alpha\alpha$	Write $\alpha\alpha$ to αLUT location 00.
.	. .	. .	. .	Repeat step 3, 254 times for locations 01h-FEh.
258	0	001	$\zeta\zeta$	Write $\zeta\zeta$, to αLUT location FF.
Read All αLUT Locations Starting from 00				
1	0	111	C6	Select αLUT and Register 06 in Address Control Register.
2	1	101	aa	Read Control Register 06.
				bb = (aa OR 20h) to set bit 5.
3	0	101	bb	Restores aa with αLUT enabled.
4	0	011	00	Write 00 into RAM Address Register (sets address to 00).
5	1	001	cc	Read contents of αLUT, cc, from location 00.
.	. .	. .	. .	Repeat step 5, 254 times for locations 01h-FEh.
260	1	001	$\zeta\zeta$	Read contents of αLUT, $\zeta\zeta$, from last location FF.

Pin Assignments

128 Pin Plastic Quad Flat Pack (PQFP) Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	D_5	33	PDA_{11}	65	R/C_R	97	M_{22}
2	D_4	34	PDA_{10}	66	B/C_B	98	M_{21}
3	D_3	35	PDA_9	67	A_{GND}	99	M_{20}
4	D_2	36	PDA_8	68	G/Y	100	M_{19}
5	D_1	37	PDA_7	69	COMP	101	M_{18}
6	D_0	38	PDA_6	70	V_{DDA}	102	M_{17}
7	$\overline{CS}$	39	PDA_5	71	V_{DDA}	103	M_{16}
8	$R/\overline{W}$	40	PDA_4	72	PDB_{23}	104	D_{GND}
9	A_0	41	PDA_3	73	PDB_{22}	105	V_{DD}
10	A_1	42	PDA_2	74	PDB21	106	M_{15}
11	A_2	43	PDA_1	75	PDB20	107	M_{14}
12	SIG0	44	PDA_0	76	PDB19	108	M_{13}
13	$\overline{PASSEN}$	45	α_8	77	PDB18	109	M_{12}
14	AV	46	α_7	78	PDB17	110	M_{11}
15	OL_3	47	V_{DD}	79	PDB16	111	M_{10}
16	V_{DD}	48	D_{GND}	80	PDB15	112	M_9
17	D_{GND}	49	α_6	81	PDB14	113	M_8
18	OL_2	50	α_5	82	PDB13	114	M_7
19	OL_1	51	α_4	83	PDB12	115	M_6
20	OL_0	52	α_3	84	PDB11	116	M_5
21	PDA_{23}	53	α_2	85	PDB10	117	M_4
22	PDA_{22}	54	α_1	86	PDB9	118	M_3
23	PDA_{21}	55	α_0	87	PDB8	119	M_2
24	PDA_{20}	56	SMX_2	88	PDB7	120	M_1
25	PDA_{19}	57	SMX_1	89	PDB6	121	M_0
26	PDA_{18}	58	SMX_0	90	PDB5	122	AVOUT
27	PDA_{17}	59	CLK	91	PDB4	123	$\overline{PASS14}$
28	PDA_{16}	60	$\overline{BLANK}$	92	PDB3	124	SIG14
29	PDA_{15}	61	$\overline{SYNC}$	93	PDB2	125	D_{GND}
30	PDA_{14}	62	V_{REF}	94	PDB1	126	V_{DD}
31	PDA_{13}	63	R_{REF}	95	PDB0	127	D_7
32	PDA_{12}	64	A_{GND}	96	M_{23}	128	D_6

Pin Descriptions

Name	Pin Number	Value	Pin Function Description
Clock			
CLK	59	TTL	**Clock Input.** TTL-compatible clock. All pixel data is registered on the rising edge of CLK. CLK synchronizes the flow of pixel data through the TMC2081 and the operation of the α-input.
Pixel I/O			
PDA_{23-0}	21-44	TTL	**A-Channel Pixel Inputs.** A-channel pixel inputs are registered on the rising edge of CLK and specify which of the CLUT locations are addressed after masking. The CLUT in the A-Channel may be bypassed. PDA_{7-0} are applied to all three CLUT sections when color-index pixel data is used.
PDB_{23-0}	72-95	TTL	**B-Channel Pixel Inputs.** B-channel pixel inputs are registered on the rising edge of CLK and are applied to the mixer after color-space conversion, and interpolation, if selected.
α_{8-0}	45,46,49-55	TTL	**α-Channel Inputs.** The α-channel inputs are registered on the rising edge of CLK and control proportional mixing at pixel rates up to 40 Mpps. α_8 acts as a key input, switching A- and B-channel pixel data on a pixel-by-pixel basis. α_0 is the LSB.
SMX_{2-0}	56-58	TTL	**ABF Crosspoint Mux Control.** When enabled by setting the SMX Control Register bits to 111, these inputs control the ABF Crosspoint Switch which directs the A- or B-channel pixels or the fill color register values to the V_1 or V_2 inputs to the mixer. SMX_{2-0} input pins are ignored when the SMX Control Register bits are not 111. SMX_{2-0} are registered on the rising edge of CLK. ABF Crosspoint Switch control is according to the following:
OL_{3-0}	15,18-20	TTL	**Overlay Inputs.** Overlay inputs select one of 15 overlay colors from the PDA overlay palette. OL_{3-0} are registered on the rising edge of CLK. When PDA or overlay is enabled and $OL_{3-0} > 0$, the contents of the addressed palette are selected in place of the pixel data. Overlay is inactive when $OL_{3-0} = 0_h$ or when disabled via the Control Registers. OL_0 is the LSB.
M_{23-0}	96-103, 106-121	TTL	**Mixed Pixel Outputs.** Mixer output or digital preview of the V_1 and V_2 Crosspoint Switch outputs are synchronized to the rising edge of CLK. M_{23-0} date is passed on for further processing (mixing, encoding, etc.). Pipeline latency is 14 clock cycles.

SMX_{2-0}	V_1	V_2
000	A	B
001	A	F
010	B	A
011	B	F
100	F	A
101	F	B
110	-	-
111	-	-

Pin Descriptions (continued)

Name	Pin Number	Value	Pin Function Description
Video Controls			
$\overline{\text{PASSEN}}$	13	TTL	**Pass Enable Input.** Data selected by A/BPASS is enabled by $\overline{\text{PASSEN}}$.
SIG0	12	TTL	**Signal 0 Input.** Input to a 14 CLK delay. Output is at SIG14.
$\overline{\text{PASS14}}$	123	TTL	**Pass Enable Output (14 Clock Delay).** $\overline{\text{PASSEN}}$ delayed by 14 CLK cycles to match the pipeline latency of pixels
SIG14	124	TTL	**Signal 0 Output (14 Clock Delay).** SIG0 delayed to match the 14 CLK cycles pipeline latency of pixels
AV	14	TTL	**Active Video Input.** When HIGH, AV enables data from the PDA and PDB ports. When LOW, at the M_{23-0} output, GBR data is set to zero and YC_BC_R data is set to 10_h 80_h 80_h in the offset binary format and 10_h 00_h 00_h in 2's complement format. In the 422 mode, AV transitioning HIGH defines the next pixel to be the first C_B pixel.
AVOUT	122	TTL	**Delayed AV Output.** AV delayed by either 12 or 14 clock cycles. A 14 clock cycle delay matches the pipeline delay of the A and B channels. A 12 clock cycle delay is useful for interfacing with Fairchild Encoders.
$\overline{\text{SYNC}}$	61	TTL	**Sync Enable for G/Y D/A.** D/A Converter sync enable. $\overline{\text{SYNC}}$= LOW, disables a current source at the G/Y output, forcing the sync tip to zero volts. $\overline{\text{SYNC}}$ = HIGH, activates the sync current at the G/Y output. $\overline{\text{SYNC}}$ is delayed either 2 or 15 clock cycles according to the status of the DACDLY bit. To disable sync on G/Y, ground $\overline{\text{SYNC}}$.
$\overline{\text{BLANK}}$	60	TTL	**Blanking Control for D/As.** D/A Converter blanking input. $\overline{\text{BLANK}}$ = LOW disables the data and pedestal output currents. If $\overline{\text{BLANK}}$ = HIGH, data and pedestal currents are added to the SYNC current. $\overline{\text{BLANK}}$ is delayed either 2 or 15 clock cycles according to the status of the DACDLY bit. For blank levels, see Tables 9, 10, 11, and 12.
Microprocessor I/O			
R/$\overline{\text{W}}$	8	TTL	**Read/Write Control.** Read-Write control input. R/$\overline{\text{W}}$ controls the direction of the D_{7-0} port. If R/$\overline{\text{W}}$ = HIGH and $\overline{\text{CS}}$ is LOW, registers or CLUTs may be read. If R/$\overline{\text{W}}$ = LOW and $\overline{\text{CS}}$ = LOW, data may be written to control registers or CLUTs via the D_{7-0} port. R/$\overline{\text{W}}$ is latched on the falling edge of $\overline{\text{CS}}$.
$\overline{\text{CS}}$	7	TTL	**Chip Select.** Chip Select Input. If $\overline{\text{CS}}$ = HIGH, port, D_{7-0}, is set to high-impedance. If $\overline{\text{CS}}$ = LOW, port D_{7-0} is enabled. Read data (R/$\overline{\text{W}}$ = HIGH) is enabled on the falling edge of $\overline{\text{CS}}$. Write data is latched into the TMC2081 on the rising edge of the $\overline{\text{CS}}$. CLUT, αLUT, or overlay read/write operations require $\overline{\text{CS}}$ to be HIGH for at least 4 CLK cycles after $\overline{\text{CS}}$ = LOW.
A_{2-0}	11-9	TTL	**Register Select Controls.** Address bits input. A_{2-0} select registers or tables to be accessed (see Table 13) via D_{7-0}. A_{2-0} are latched on the falling edge of $\overline{\text{CS}}$.
D_{7-0}	127,128, 1-6	TTL	**Data I/O Port.** Bi-directional data port. D_0 is the LSB. Control Registers, CLUT, αLUT and Overlay locations are accessed via D_{7-0}.
Video Output			
G/Y	68	1 V P-P	**Green/Luminance Video.** The green/luminance analog video output. Sync pulses are included on this output.
B/C_B	66	0.7 V P-P	**Blue/C_B Video.** Blue/C_B analog video output.
R/C_R	65	0.7 V P-P	**Red/C_R Video.** Red/C_R analog video output.

Pin Descriptions (continued)

Name	Pin Number	Value	Pin Function Description
Reference			
V_{REF}	62	+1.23 V	**Voltage Reference Input/Output.** An internal voltage source of +1.2 Volts (nominal) is applied to the V_{REF} terminal. This is the reference for all three D/A converters of the TMC2081. Decoupling V_{REF} to A_{GND} with a 0.1μF ceramic capacitor is recommended. This pin may also be used as an input for an external voltage reference source.
R_{REF}	63	681 Ω	**Current-Setting Resistor.** Full-scale output current of the TMC2081 is determined by the value of the resistor connected between R_{REF} and A_{GND}. Varying this resistor will vary the “white” output level for all three D/A converters. The TMC2081 is not designed for operation with an external current reference.
COMP	69	0.1 μF	**Compensation Capacitor.** A 0.1 μF ceramic capacitor is connected between the COMP and V_{DDA} at pin 70 or 71.
Power, Ground			
V_{DDA}	70,71	+5 V	**Analog Power Supply.** The TMC2081 operates from a single +5V supply. All power pins must be connected. V_{DDA} and V_{DD} must be derived from a common power supply.
V_{DD}	16,47,105,126	+5 V	**Digital Power Supply.** The TMC2081 operates from a single +5V supply. All power pins must be connected. V_{DDA} and V_{DD} must be derived from a common power supply.
A_{GND}	64,67	0.0 V	**Analog Ground.** All ground pins must be connected.
D_{GND}	17,48,104,125	0.0 V	**Digital Ground.** All ground pins must be connected.

Control Register Map

Reg	Bit	Name	Function
A-Channel Control Register			
00	7	AOVLEN	A-channel Overlay enable/disable
00	6	ADEC	Decimator bypass/enable
00	5	AMAT	A-channel GBR-to-YC_BC_R bypass/enable
00	4	CLUT	Bypass/enable CLUT (power down)
00	3	AMSB	Inverts C_B/C_R MSB
00	2	αGAIN	Alpha Channel 9-/8-bit gain
00	1-0	AFORMAT	A Pixel data path setup (4 formats)
B-Channel/Mixer Control Register			
01	7		Reserved
01	6-5	MSOURCE	M_{23-0} pixel source
01	4	BMAT	Bypass/enable the B-channel YC_BC_R-to-GBR
01	3	BINT	Bypass/enable Interpolator
01	2	BMSB	Inverts C_B/C_R MSB
01	1-0	BFORMAT	B Pixel data path setup (4 formats)
Mixer Control Register			
02	7	MIXFMT	Mixer format select
02	6-5	DSOURCE	Selects data source for the internal D/A converters
02	4-2	SMX	Chooses video source to be directed to the mixer imputs, V_1 and V_2
02	1-0	MIXTFN	Used to alter the mixer transfer function
Fill Color Registers			
03	7-0	REDVAL	Value for Red/C_R
04	7-0	GRNVAL	Value for Green/Y
05	7-0	BLEVAL	Value for Blue/C_B

Reg	Bit	Name	Function
Output Control Register			
06	7	AVPIPE	Sets pipeline latency of AV
06	6		Reserved
06	5	αLUTEN	αLUTEN power down enable
06	4	PASSON	Sets pixel activity subject to mixer transfer function
06	3	A/BPASS	Selects A or B data in PASSON mode
06	2	MOUT	Bits M_{23-0} enable
06	1	MMSB	Inverts C_B, C_R MSBs
06	0	MFORMAT	Sets output data format
D/A Control Register			
07	7-6		Reserved
07	5	DACDLY	Selects SYNC and BLANK pipe delay
07	4	DACFMT	C_B/C_R translate from 2's complement to offset binary
07	3	AWAKE	D/A converters enable/ disable
07	2	SETUP	Sets IRE blanking levels
07	1		Reserved
07	0	DMAT	D/A converter input data YC_BC_R/GBR conversion
Identification (read-only)			
08	7-0	REVID	Chip revision ID
09	7-0	CHIPID	Chip type ID = 2F

Control Register Definitions

A-Channel Control Register (00)

7	6	5	4	3	2	1	0
AOVLEN	ADEC	AMAT	CLUT	AMSB	αGAIN	AFORMAT	

Reg	Bit	Name	Description
00	7	AOVLEN	When HIGH, the Overlay palette in the PDA pixel path is enabled and controlled by the OL_{3-0} inputs. When LOW, the PDA Overlay palette is disabled.
00	6	ADEC	When HIGH, this bit causes A-channel pixel data to be decimated from YC_BC_R444 to YC_BC_R422 format. When LOW, no decimation takes place and the data is passed through.
00	5	AMAT	When HIGH, the A-channel pixel data is converted from GBR to YC_BC_R format. When LOW, no conversion takes place and the data is passed through.
00	4	CLUT	When HIGH, the A-channel CLUT is enabled and addressed by pixel data. When LOW the CLUT is bypassed.
00	3	AMSB	When LOW,the MSBs of the A-channel C_B and C_R (PDA_{15} and PDA_7) are passed though. When HIGH, the MSBs of the C_B and C_R are inverted.
00	2	αGAIN	α-channel gain. LOW selects 9-bit unity gain. HIGH selects 8-bit gain. For 8-bit α mixing, set $\alpha_8 = 0$.
00	1-0	AFORMAT	These two bits set up the A channel data path to accommodate four different formats: 0 0 YC_BC_R444 0 1 YC_BC_R422 1 0 8-bit color index 1 1 24-bit GBR

Control Register Definitions (continued)

B-Channel Control Register (01)

7	6	5	4	3	2	1	0
Reserved	MSOURCE		BMAT	BINT	BMSB	BFORMAT	

Reg	Bit	Name	Description
01	7		Reserved.
01	6-5	MSOURCE	Source of pixels to be connected to port M_{23-0}. 0 0 Mixer Pixels 0 1 A pixels 1 0 B pixels 1 1 Reserved
01	4	BMAT	When HIGH, the B-channel pixel data is converted from YC_BC_R to GBR format. When LOW, no conversion takes place and the data is passed through.
01	3	BINT	When HIGH, B-channel pixel data is interpolated from the YC_BC_R422 to the YC_BC_R444 format. When LOW, no interpolation takes place and the data is passed through.
01	2	BMSB	When LOW, the MSBs of the B-channel C_B and C_R bytes (PDB_{15} and PDB_7) are passed through. When HIGH, the MSBs of the C_B and C_R bytes are inverted.
01	1-0	BFORMAT	B-channel pixel data format select bits. 0 0 YC_BC_R444 0 1 YC_BC_R422 1 0 Reserved 1 1 24-bit GBR

Control Register Definitions (continued)

Mixer Control Register (02)

7	6	5	4	3	2	1	0
MIXFMT	DSOURCE		SMX			MIXFTN	

Reg	Bit	Name	Description
02	7	MIXFMT	When LOW, the mixer is set for YC_BC_R format. When HIGH, the mixer expects GBR format.
02	6-5	DSOURCE	The data source for the internal D/A converters is selected by two control bits. 0 0 A-pixels 0 1 B-pixels 1 0 Mixed pixels 1 1 Reserved
02	4-2	SMX	These three control bits determine which video sources (A-pixels, B-pixels, fill color registers) are directed to the two mixer inputs, V_1 and V_2, through the ABF Crosspoint Mux: 0 0 0 A to V_1, B to V_2 0 0 1 A to V_1, F to V_2 0 1 0 B to V_1, A to V_2 0 1 1 B to V_1, F to V_2 1 0 0 F to V_1, A to V_2 1 0 1 F to V_1, B to V_2 1 1 0 Reserved 1 1 1 Enables SMX_{2-0} inputs for external source select
02	1-0	MIXTFN	These two bits are used to alter the mixer transfer function: 0 0 $(V_1 – V_2)\alpha + V_2$ 0 1 $(V_1)\ \alpha + V_2$ 1 0 $(V_1)\ \alpha$ 1 1 Reserved

Fill Color Registers (03–05)

Reg	Bit	Name	Description
03	7-0	REDVAL	Value for Red/C_R
04	7-0	GRNVAL	Value for Green/Y
05	7-0	BLUVAL	Value for Blue/C_B

Control Register Definitions (continued)

Output Control Register (06)

7	6	5	4	3	2	1	0
AVPIPE	Reserved	αLUTEN	PASSON	A/BPASS	MOUT	MMSB	MFORMAT

Reg	Bit	Name	Description
06	7	AVPIPE	When LOW the pipeline latency from AV, to AVOUT is 14 CLK cycles. When HIGH, the pipeline latency is 12 CLK cycles.
06	6		Reserved.
06	5	αLUTEN	When LOW (write only), the αLUTEN is powered down. Data from α_{8-0} bypasses the αLUT to control the mixer directly. When HIGH, α_{7-0} addresses the αLUT which controls the mixer.
06	4	PASSON	When HIGH, either PDA or PDB data may be selected to pass through the mixer without modification. When LOW the mixer transfer function is enabled if the $\overline{\text{PASSEN}}$ input is HIGH. The PASSON feature allows Genlock or Decoder reference signals to be passed downstream for subsequent processing.
06	3	A/BPASS	Selects A or B data in PASSON mode. LOW allows all pixels from PDA_{23-0} during $\overline{\text{PASSEN}}$ = LOW to pass to M_{23-0}. HIGH allows all pixels from PDB_{23-0} during $\overline{\text{PASSEN}}$ = LOW to pass to M_{23-0}.
06	2	MOUT	Digital outputs M_{23-0} are enabled when this bit is HIGH. These outputs are in a high-impedance state when MOUT is LOW.
06	1	MMSB	When LOW, the MSBs of the C_B and C_R M_{23-0} output positions (M_{15} and M_7) are not inverted. When HIGH, the MSBs of the C_B and C_R output positions are inverted.
06	0	MFORMAT	When LOW, 24-bit GBR or YC_BC_R444 output data formats are enabled. When HIGH, the multiplexer in the M_{23-0} path is enabled producing 16-bit YC_BC_R422.

D/A Control Register (07)

7	6	5	4	3	2	1	0
Reserved		DACDLY	DACFMT	AWAKE	SETUP	DOVLEN	DMAT

Reg	Bit	Name	Description
07	7-6		Reserved.
07	5	DACDLY	Selects $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ pipe delay. LOW = 15 clocks, HIGH = 2 clocks.
07	4	DACFMT	Translates C_B/C_R format from 2's complement to C_B/C_R offset binary. LOW passes C_B/C_R unchanged. HIGH inverts C_B/C_R MSB.
07	3	AWAKE	D/A converters are enabled when HIGH. The D/A converters are powered-down when AWAKE is LOW.
07	2	SETUP	When LOW, 0 IRE blanking levels are present on the D/A converter outputs. When HIGH, blanking levels are 7.5 IRE units.
07	1		Reserved.
07	0	DMAT	When HIGH, D/A converter input data is converted from YC_BC_R to GBR format. When LOW, no conversion takes place and the data is passed through.

Control Register Definitions (continued)

Identification Registers (08-09)

Reg	Bit	Name	Description
08	7-0	REVID	Chip revision identification.
09	7-0	PARTID	Chip type identification = 2F.

Absolute Maximum Ratings
(beyond which the device may be damaged)[1]

Parameter	Min.	Max.	Unit
Power Supply Voltage	-0.5	+7.0	V
Input Voltage	-0.5	(V_{DD} + 0.5)	V
Digital Inputs			
Applied voltage[2]	-0.5	(V_{DD}+ 0.5)	V
Externally forced current [3, 4]	-20.0	20.0	mA
Digital Outputs			
Applied voltage[2]	-0.5	(V_{DD}+ 0. 5)	V
Externally forced current[3, 4]	-20.0	20.0	mA
Short Circuit Duration (Single output in HIGH state to GND)		1 second	
Analog Output Short Circuit Duration (Single output to GND)		infinite	
Temperature			
Operating, case	-60	+130	°C
Operating, Junction, Plastic package		+150	°C
Lead, soldering (10 seconds)		300	°C
Vapor phase soldering (1 minute)		+220	°C
Storage	-65	150	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Min.	Nom	Max.	Units
V_{DD}	Power Supply Voltage	4.75	5.0	5.25	V
V_{IH}	Input Voltage, Logic HIGH				
	TTL Inputs, all but CLK, $\overline{CE}$	2.0		V_{DD}	V
	CLK, $\overline{CE}$	2.4		V_{DD}	V
V_{IL}	Input Voltage, Logic LOW				
	TTL Inputs	GND		0.8	V
I_{OH}	Output Current, Logic HIGH			-2.0	mA
I_{OL}	Output Current, Logic LOW			4.0	mA
V_{REF}	External Reference Voltage		1.235		V
I_{REF}	D/A Converter Reference Current		1.8		mA
	($I_{REF} = V_{REF} / R_{REF}$, sourced from R_{REF} pin)				
R_{REF}	Reference Resistor @ V_{REF} = Nom.		681		Ω
R_{OUT}	Total Output Load Resistance		37.5		Ω
T_A	Ambient Temperature, Still Air	0		70	°C

Electrical Characteristics

Parameter		Conditions	Min.	Typ.	Max.	Units
I_{DD}	Power Supply Current[1]	f_{CLK} = 25MHz, DAC, CLUT and αLUT enabled		300	360	mA
I_{DDQ}	Power Supply Current[1]	f_{CLK} = 0 DAC, CLUT and αLUT enabled		260	330	mA
I_{DAC}	DAC Supply Current	f_{CLK} = 25MHz		80	100	mA
I_{CLUT}	CLUT Supply Current			85	100	mA
$I_{\alpha LUT}$	αLUT Supply Current			30	45	mA
I_{DDSE}	Power Supply Current	Sleep Mode (D/A, CLUT, αLUT, and D/A overlay disabled)		5	15	mA
V_{RO}	Voltage Reference Output		0.98	1.2	1.48	V
I_{BR}	Input Bias Current, V_{REF}	V_{REF} = Nom	-100		40	µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = 4.0V	-5		5	µA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0.4V	-5		5	µA
V_{OH}	Output Voltage, Logic HIGH	I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, Logic LOW	I_{OL} = Max			0.4	V
I_{OZH}	High-Z Leakage Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}	-5		5	µA
I_{OZL}	High-Z Leakage Current, LOW	V_{DD} = Max, V_{IN} = GND	-5		5	µA
C_I	Digital Input Capacitance	T_A = 25°C, f = 1MHz		15		pF
C_O	Digital Output Capacitance	T_A = 25°C, f = 1MHz		15		pF
V_{OC}	Video Output Compliance Voltage		-0.4		2.0	V
R_{OUT}	Video Output Resistance			15		KΩ
C_{OUT}	Video Output Capacitance	I_{OUT} = 0mA, f = 1MHz		15	25	pF

Note:

1. Typical I_{DD} measured at V_{DD} = +5.0 Volts and T_A = 25°C, Maximum I_{DD} measured at V_{DD} = + 5.25 Volts and T_A = 0°C.

Switching Characteristics

Parameter		Min.	Nom.	Max.	Units
Microprocessor Interface					
t_{PWLCS}	$\overline{CS}$ Pulse Width, LOW	95			ns
t_{PWHCS}	$\overline{CS}$ Pulse Width, HIGH		$4/f_{PXL}$		ns
t_{SA}	Address Setup Time	0			ns
t_{HA}	Address Hold Time	4			ns
t_{SD}	Data Setup Time (write)	6			ns
t_{HD}	Data Hold Time (write)	3			ns
t_{DOZ}	Output Delay, $\overline{CS}$ to low-Z	16			ns
t_{DOM}	Output Delay, $\overline{CS}$ to Data Valid			110	ns
t_{HOM}	Output Hold Time, $\overline{CS}$ to High-Z	7			ns
Pixel Interface					
f_{PXL}	Pixel Rate			40	Mpps
t_{CYPX}	Pixel Cycle Period	25			ns
t_{PWH}	CLK Pulse Width, HIGH	6			ns
t_{PWL}	CLK Pulse Width, LOW	6			ns
	For PDA, PDB, α, SMX, OL, $\overline{PASSEN}$, SIG0, AV inputs:				
t_{SP}	Setup Time	6			ns
t_{HP}	Hold Time	2			ns
t_{HO}	Output Hold Time, CLK to data disabled	6			ns
t_{DO}	Output Delay, CLK to data valid			17	ns
Analog Outputs					
PIPES	Pipeline Delay		15		CLKs
t_R	D/A Output Current Risetime (10% - 90%)		6		ns
t_F	D/A Output Current Falltime (10% - 90%)		3		ns
t_{DOV}	Analog Output Delay		20		ns
SKEW	D/A to D/A Output Skew			1	ns

Notes:

1. Timing reference points are at the 50% level.
2. Analog and digital C_{LOAD} = 15pF.
3. TTL input levels are 0.0 and 3.0 Volts, 10% - 90% rise and fall times < ns.

System Performance Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
V_{VID}	Video Amplitude with 37.5 Ω load		0.7		Volt
V_{SYNC}	Sync Amplitude with 37.5 Ω load		0.3		Volt
RES	D/A Converter Resolution		8		Bits
E_{LI}	D/A Integral Linearity Error			0.75	LSB
E_{LD}	D/A Differential Linearity Error			0.75	LSB
E_G	D/A Gain Error			±11	% FS

Timing Diagrams

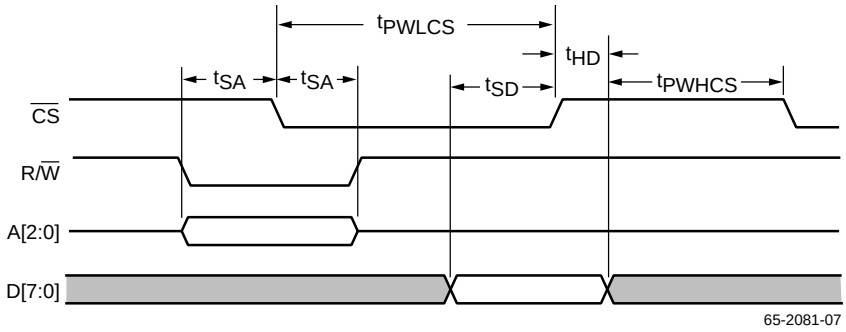


Figure 4. Microprocessor Port Write Timing

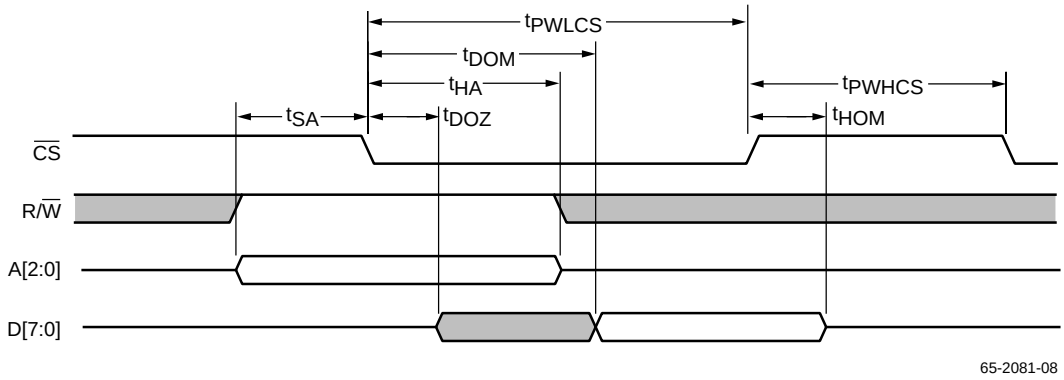


Figure 5. Microprocessor Port Read Timing

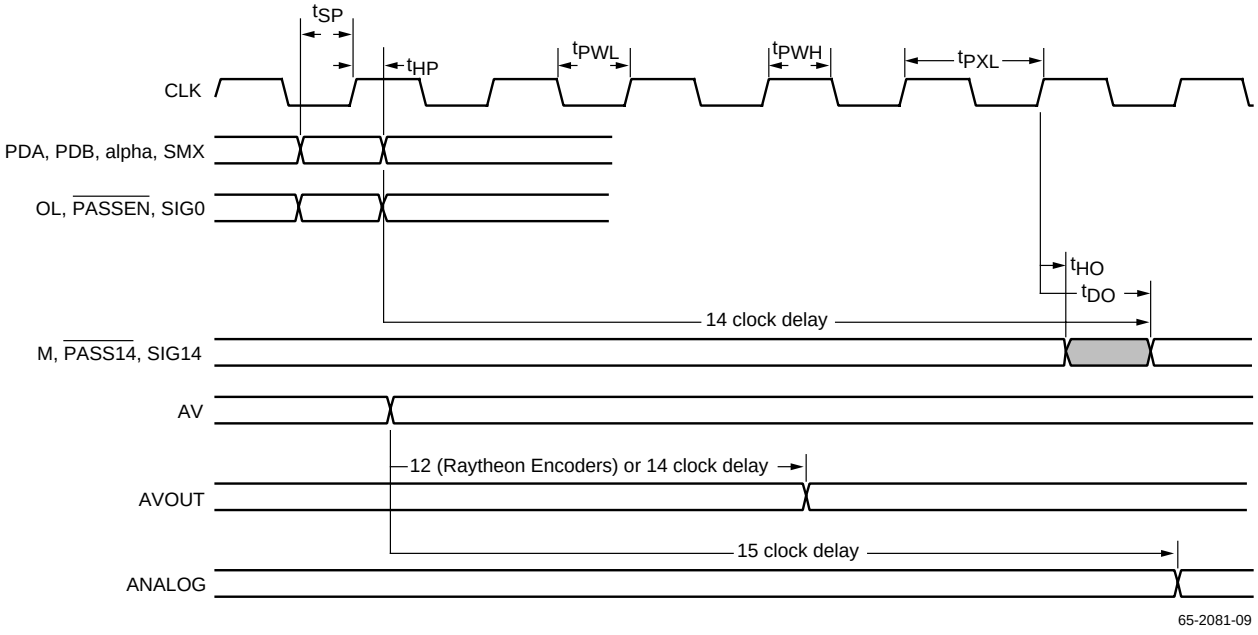


Figure 6. Pixel Timing

Timing Diagrams (continued)

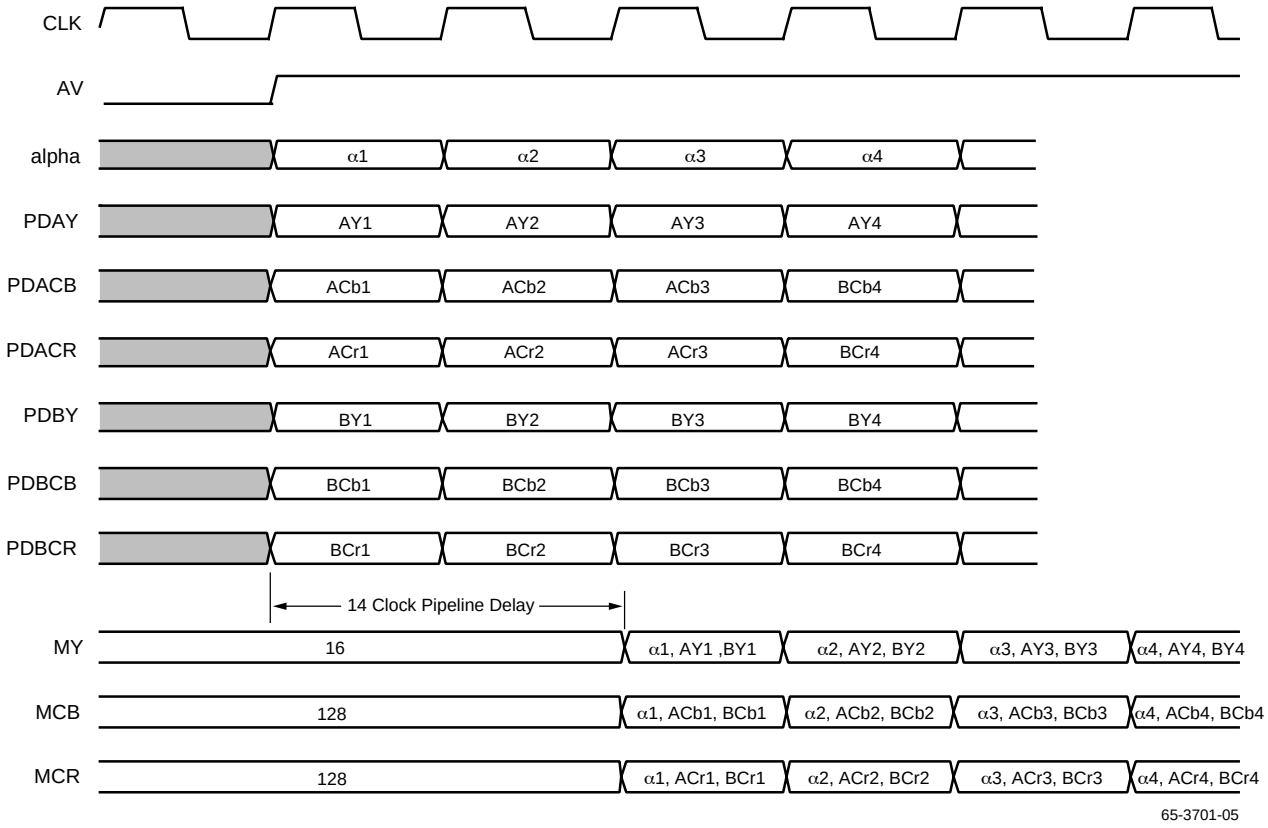


Figure 7. Pixel/Alpha Data Timing – 444/444 Mode

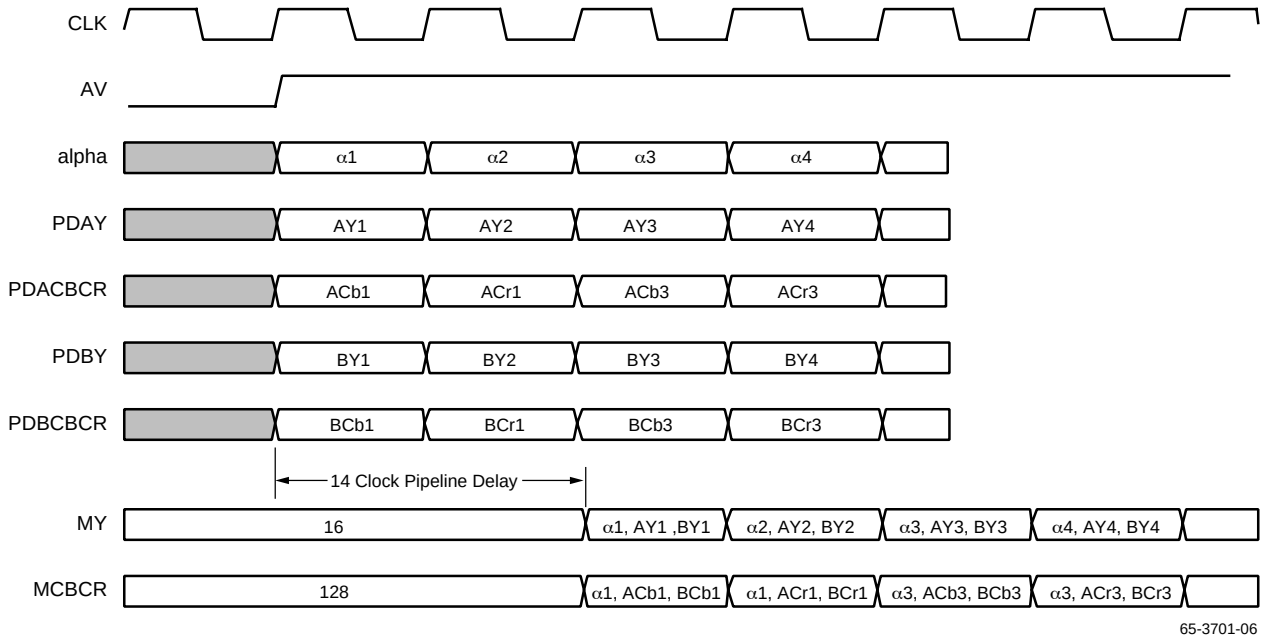


Figure 8. Pixel/Alpha Data Timing – 422/422 Mode

Timing Diagrams (continued)

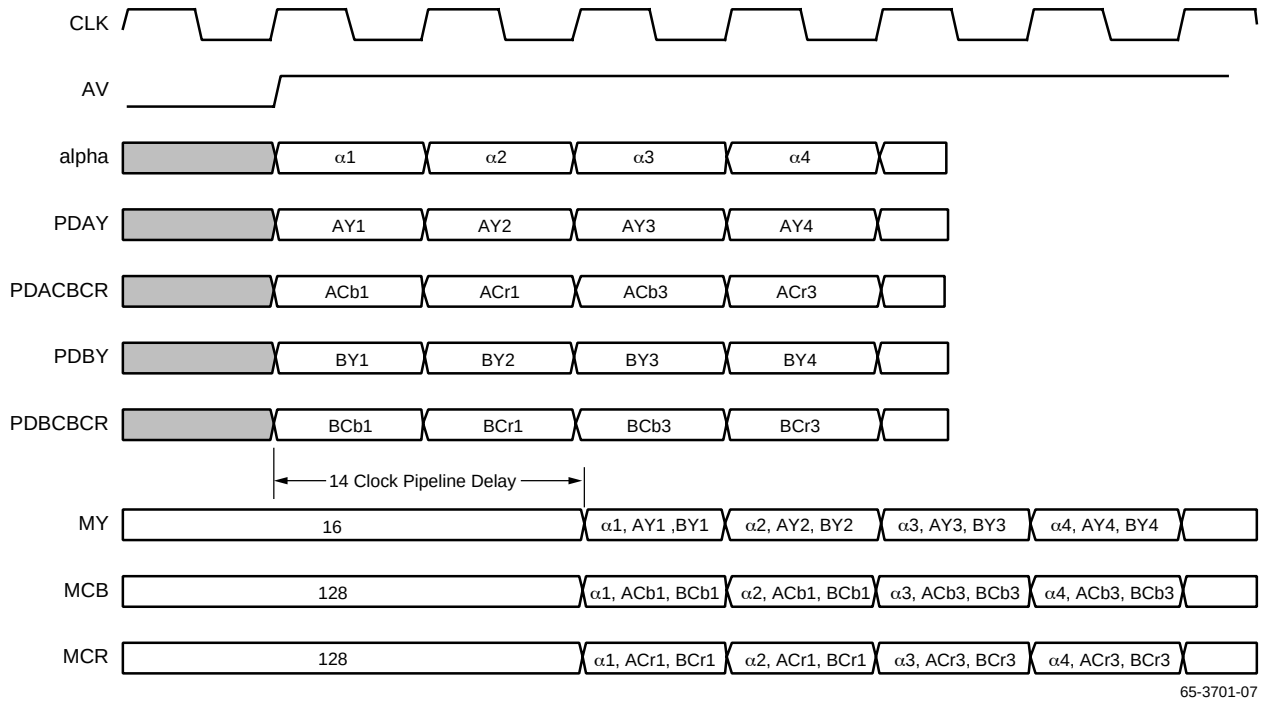


Figure 9. Pixel/Alpha Data Timing – 422/444 Mode

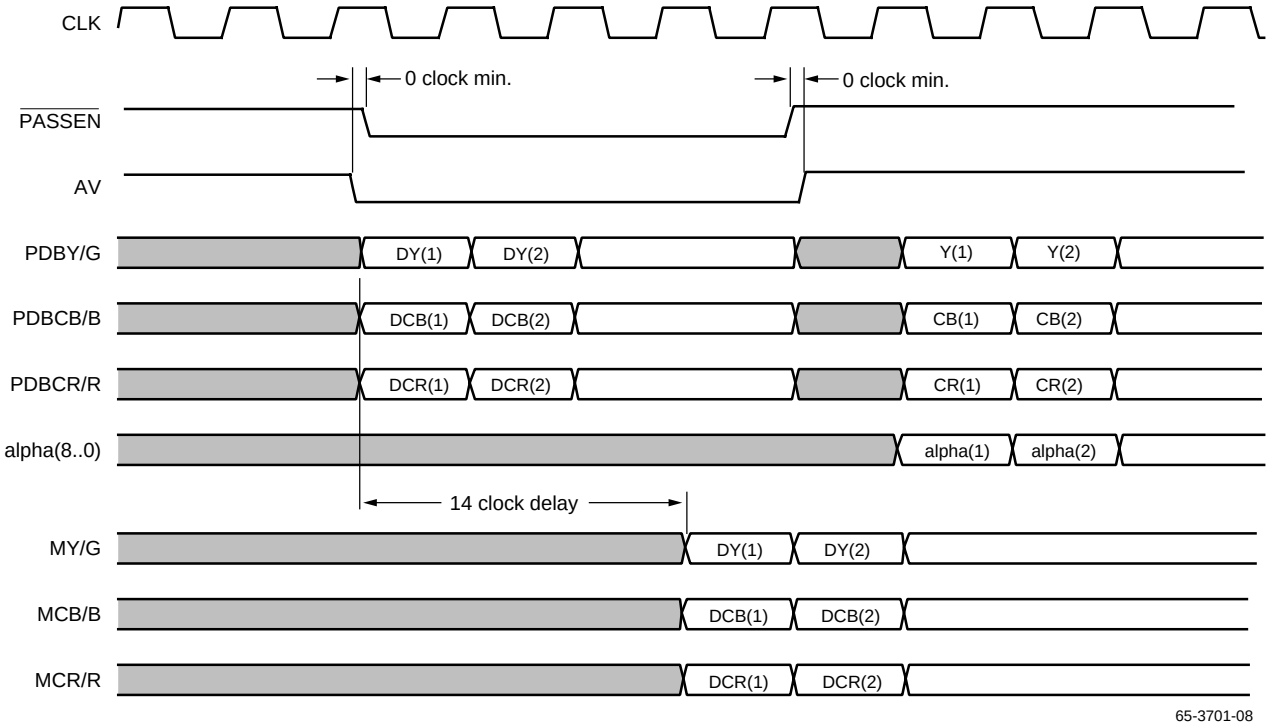


Figure 10. PASSON Timing – 444 Mode
(Control bits: PASSON = HIGH, A/BPASS = HIGH)

Timing Diagrams (continued)

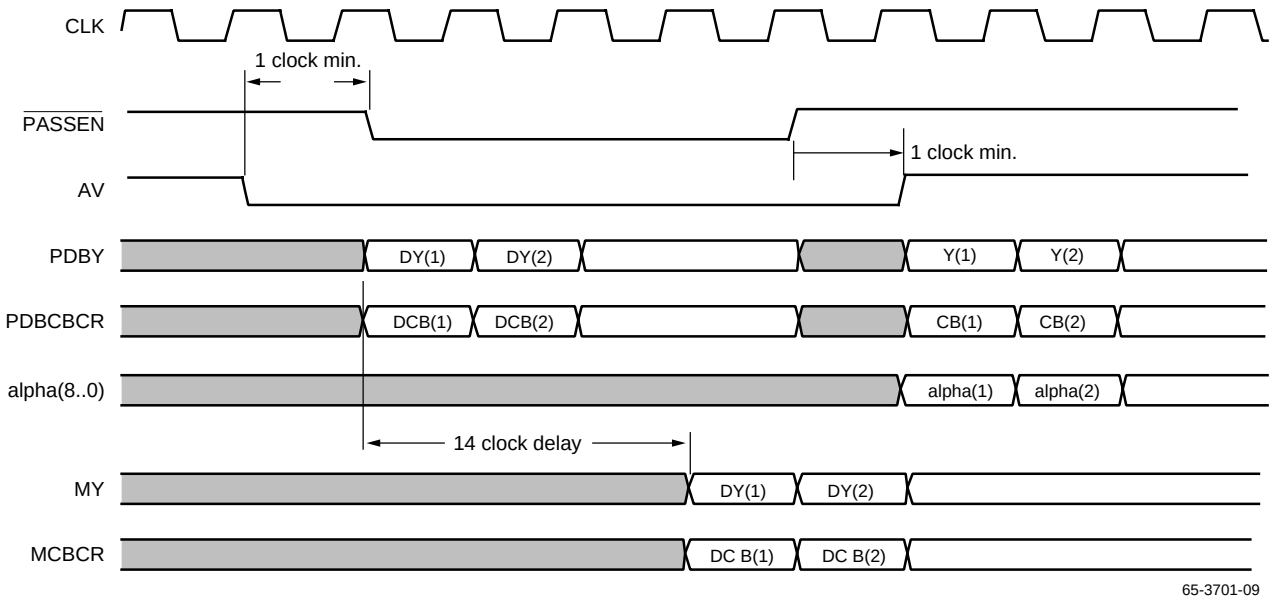


Figure 11. PASSON Timing – 422 mode
(Control bits: PASSON = HIGH, A/BPASS = HIGH)

Equivalent Circuits

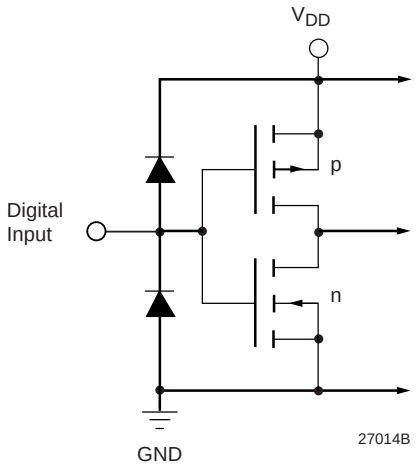


Figure 12. Equivalent Digital Input Circuit

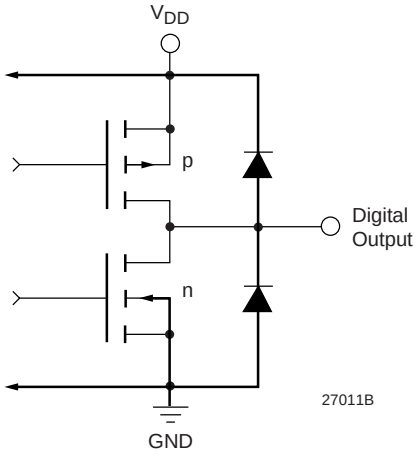


Figure 13. Equivalent Digital Output Circuit

Equivalent Circuits (continued)

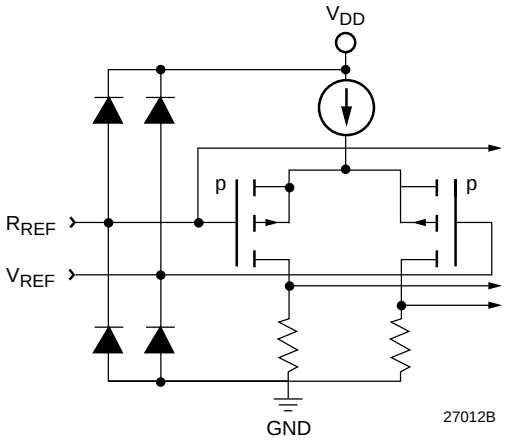


Figure 14. Equivalent Analog Input Circuit

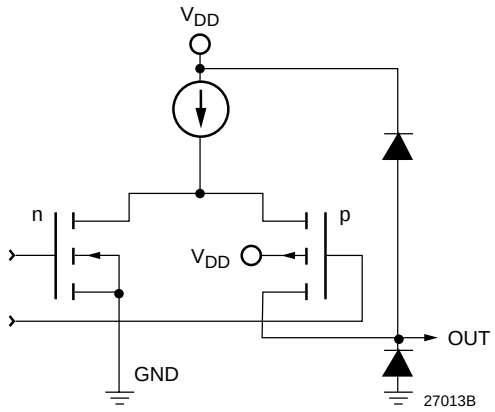


Figure 15. Equivalent Analog Output Circuit

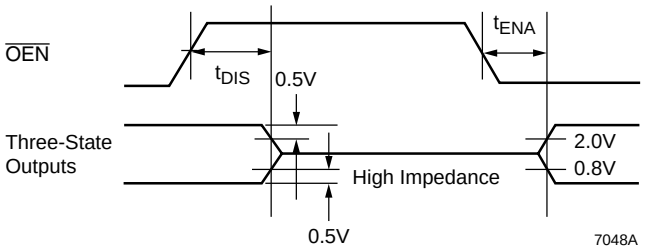


Figure 16. Threshold Levels for Three-State Measurement

Application Information

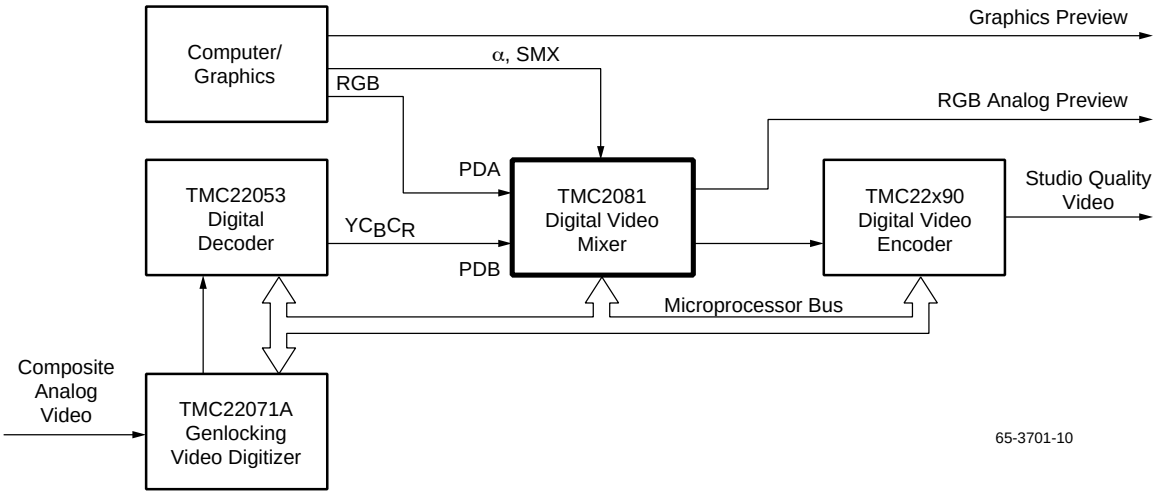


Figure 17. Mixing Video and Computer Graphics – Basic Multimedia System

Application Notes (continued)

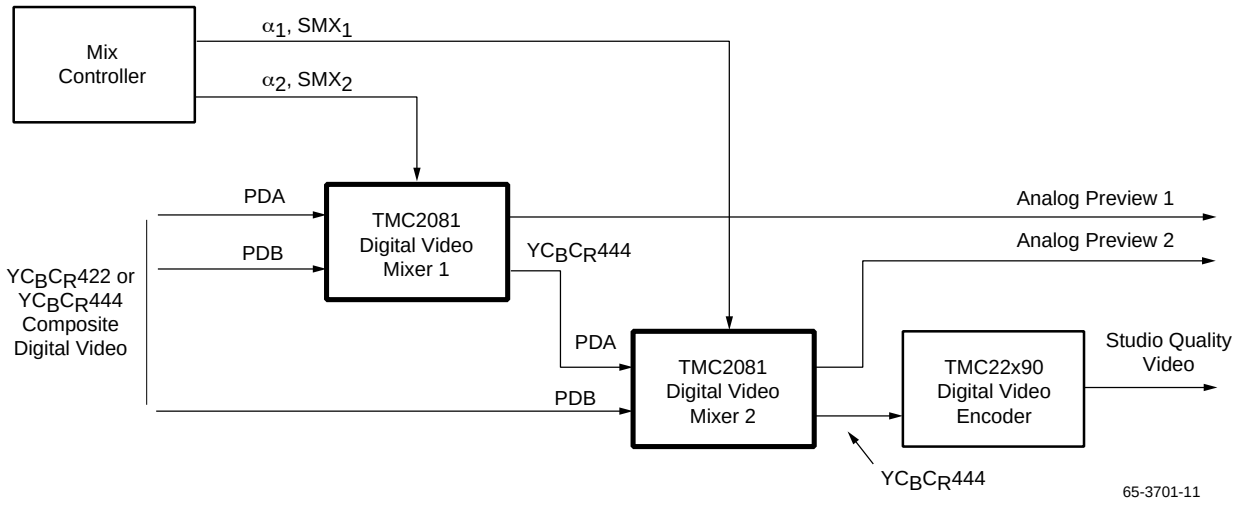


Figure 19. Multilevel Video Mixer with Special Effects

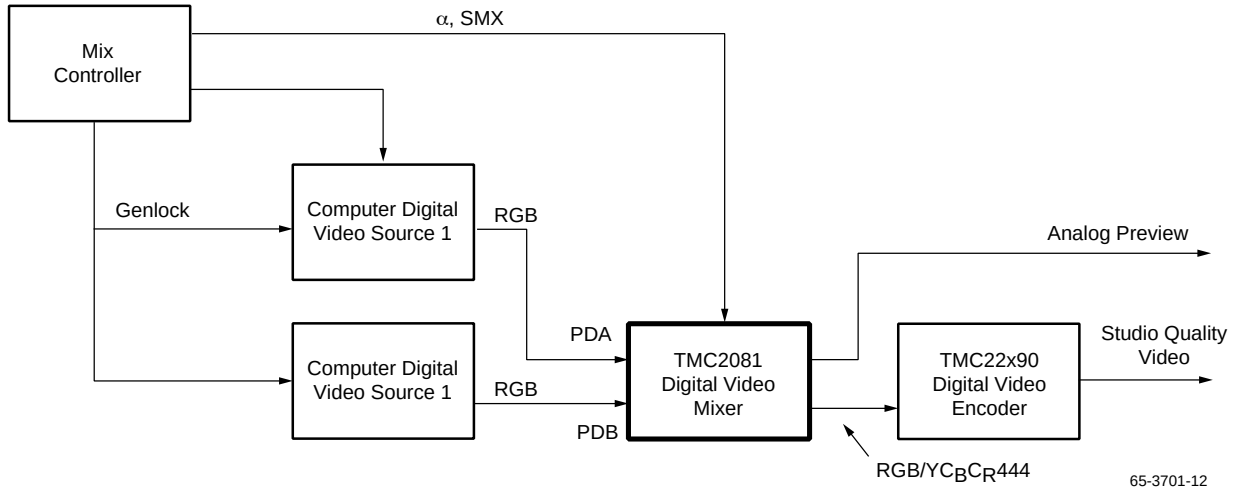


Figure 20. Mixing Two Computer Graphics Sources

Application Notes (continued)

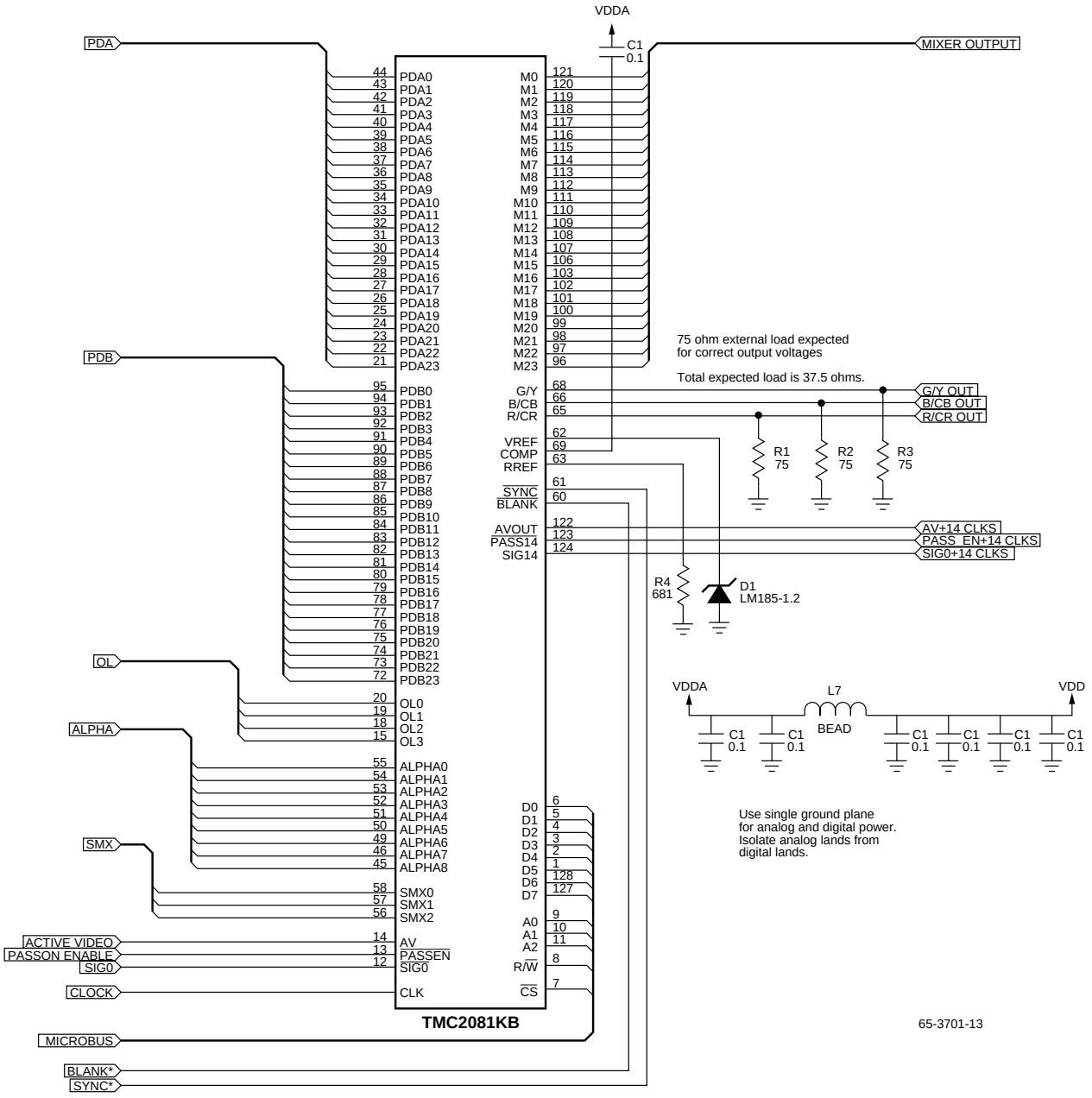


Figure 21. Recommended TMC2081 Connections

Related Products

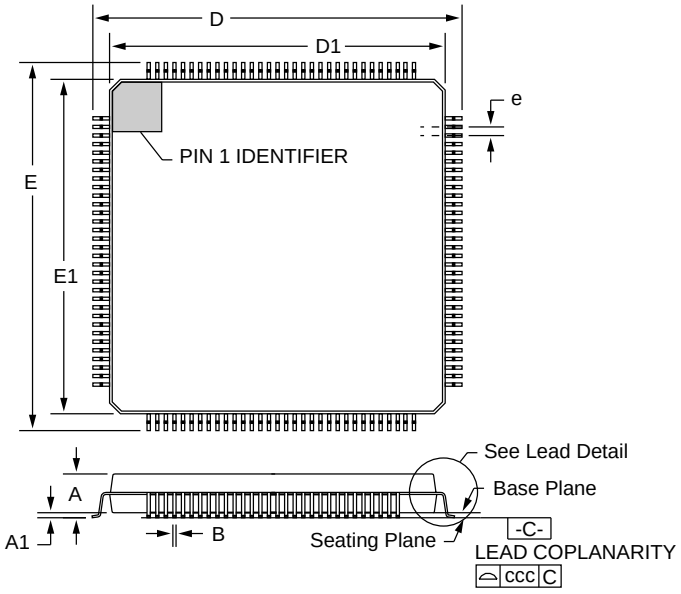
- TMC2072 Genlocking Video Digitizer
- TMC22190/191 Digital Video Encoder
- TMC2242A/TMC2246A Digital Filter
- TMC2272A Color Space Converter
- TMC22053 Decoder

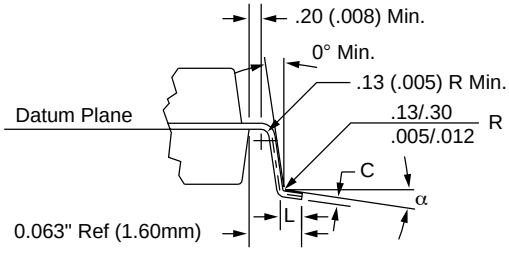
Mechanical Dimensions – 128-Lead MQFP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.160	—	4.07	
A1	.010	—	.25	—	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D/E	1.219	1.238	30.95	31.45	
D1/E1	1.098	1.106	27.90	28.10	
e	.0315 BSC		.80 BSC		
L	.029	.041	.73	1.03	4
N	128		128		
ND	32		32		
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.





Lead Detail

Notes:

Notes:

Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2081KBC	T_A = 0°C to 70°C	Commercial	128-Lead MQFP	2081KBC

5/20/98 0.0m 001
Stock# DS70002081